Electronic Version
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Claims

[c1] 1. A high-voltage metal-oxide-semiconductor (HV-MOS) device, comprising:
a substrate;
a gate dielectric layer on the substrate;
a gate on the gate dielectric layer;
a channel region in the substrate under the gate dielectric layer;
two doped regions as a source and a drain in the substrate beside the gate;
a field isolation layer between the gate and at least one of the doped regions;
a drift region in the substrate under the field isolation layer, connecting with the channel region and the at least one doped region; and
a modifying doped region in the substrate at periphery of the at least one doped region.

[c2] 2. The HV-MOS device of claim 1, wherein the field isolation layer is between the gate and the two doped regions, and the modifying doped region is in the substrate at the peripheries of the two doped regions.

[c3] 3. The HV-MOS device of claim 1, wherein the drift re-

gion and the modifying doped region together completely surround the at least one doped region.

[c4] 4. The HV-MOS device of claim 1, wherein the field isolation layer comprises a field oxide (FOX) layer.

[c5] 5. The HV-MOS device of claim 1, wherein each doped region comprises a heavily doped contact region and a lightly doped grade region under the contact region.

[c6] 6. The HV-MOS device of claim 1, wherein a doping concentration of the drift region and the modifying doped region ranges from $5\times10^{15}/cm^3$ to $5\times10^{17}/cm^3$.

[c7] 7. A method for fabricating a high-voltage metal-oxide-semiconductor(HV-MOS) device, comprising:
forming a patterned first mask layer on a substrate, having a first part covering a channel region in the substrate and two second parts beside the first part covering two regions of the substrate predetermined for a source and a drain, respectively, wherein the first part is apart from at least one of the two second parts;
forming a patterned second mask layer over the substrate, having an opening therein exposing the substrate between the first part and the at least one second part of the first mask layer and exposing another portion of the substrate at periphery of the at least one second part of

the first mask layer;
implanting a dopant into the substrate using the first and second mask layers as a mask to form doped regions in the exposed portions of the substrate;
removing the second mask layer;
forming a field isolation layer on the substrate using the first mask layer as a mask, while the doped region under the field isolation layer between the first part and the at least one second part of the first mask layer serves as a drift region, and the doped region under the field isolation layer at the periphery of the at least one second part of the first mask layer serves as a modifying doped region;
removing the first mask layer;
forming a gate dielectric layer and a gate covering the channel region; and
forming a source region and a drain region in the substrate beside the gate using the gate and the field isolation layer as a mask.

[c8] 8. The method of claim 7, wherein the first part of the first mask layer is apart from the two second parts of the first mask layer, and the opening in the second mask layer exposes the substrate between the first part and the two second parts of the first mask layer and exposes another portion of the substrate at the peripheries of the

two second parts of the first mask layer.

[c9] 9. The method of claim 7, wherein the opening in the second mask layer exposes a portion of the substrate completely surrounding the at least one second part of the first mask layer.

[c10] 10. The method of claim 7, wherein the step of forming the field isolation layer comprises:
performing a thermal oxidation process to form a field oxide (FOX) layer on the substrate using the first mask layer as a mask.

[c11] 11. The method of claim 7, wherein the step of forming the source region and the drain region comprises:
forming two heavily doped contact regions in the substrate beside the gate using the gate and the field isolation layer as a mask; and
forming two lightly doped grade regions in the substrate beside the gate using the gate and the field isolation layer as a mask, wherein the grade regions are formed deeper than the contact regions.

[c12] 12. The method of claim 7, wherein the step of implanting the dopant into the substrate is performed in a dosage ranging from $10^{12}/cm^2$ to $10^{14}/cm^2$.

[c13] 13. The method of claim 7, wherein the first mask layer

comprises SiN.

[c14] 14. The method of claim 7, wherein the second mask layer comprises a patterned photoresist layer.